Amendments to the Specification

Please modify paragraphs [0015], [0022], [0028], [0029], [0031], [0032], [0040], [0042], and [0043] as follows:

[0015] These and other advantages and features will become readily apparent in view of the following detailed description of the invention.

[0022] FIG. 1 illustrates a conventional first order RC low-pass filter 100 (e.g., an inverting integrator). The filter 100 receives an input signal (V_{IN}) at a resistor 102, which in turn is coupled to an inverting input of an operational amplifier 104. A non-inverting input of the operational amplifier 104 is coupled to ground. A capacitor 106 is coupled between the inverting input of operational amplifier 104 and its output node. The circuit produces an output signal (V_{OUT}). The first order RC low-pass filter corner frequency is set by $1/(2\pi RC)$.

[0028] Turning now to the present invention, FIG. 4 illustrates an active low-pass filter and ~~caparator~~ comparator circuit for achieving accurate filtering on an integrated circuit. In order to overcome manufacturing process variations and errors introduced by temperature variations, the inventors have combined an active low-pass filter 402 (e.g., an inverting integrator) with a tuning circuit 404 in order to accurately adjust the corner frequency of the low-pass filter 402. In general, the tuning circuit 404 generates a control signal 406 to adjust two variable resistors (416 (e.g., resistor R_{ADJ})and 420(e.g., resistor R). Variable resistor 416 in the tuning circuit 404 and variable resistor 420 in the active low-pass filter 402 are identical and are adjusted by control signal 406 as a function of the equivalent resistance of a switched-capacitor 408 and the VADJ/VREF ratio that determines the corner frequency of the low-pass filter 402.

[0029] Specifically, tuning circuit 404 comprises switched capacitor 408, an amplifier 410, a comparator 412 (e.g., an operational amplifier), a successive approximation

register (SAR) architecture analog-to-digital converter 414 and a variable resistor 416. An adjustable voltage (VADJ) is applied to an input of the switched-capacitor 408. An output of switched-capacitor 408 is coupled to an inverting input of amplifier 410. A non-inverting input of amplifier 410 is coupled to ground. An output of amplifier 410 is coupled to an inverting input of a comparator 412.

[0031] The active low-pass filter (LPF) 402 comprises a variable resistor 420, a capacitor 422 and an amplifier 424 (e.g., an operational amplifier). A signal to be filtered is applied to a first node label VIN, which is coupled to resistor 420. Resistor 420 also coupled to the inverting input of amplifier 424. A non-inverting input of amplifier 424 is coupled to ground. Capacitor 422 is coupled across the inverting input of amplifier 424 and its output node, which is labeled as VOUT. Variable resistor 420 also receives control signal 406 to change its resistance value.

[0032] Operation of the tuning circuit 404 in FIG. 4 will be described next. To illustrate the operation of tuning circuit 404, ~~consider a case in which~~ assume voltages VADJ and VREF are kept constant. Also, for this explanation, assume comparator 412 and ~~successive approximation register (SAR)~~ A/D converter 414 simply comprise ~~an amplifier~~ a comparator 430 that produces the control signal 406 to adjust resistor 416. In ~~the simple~~ this case, the comparator 430 will produce a control signal 406 to adjust resistor 416 to match the value of resistor 408 until the output voltage of amplifier 410 is equal to VREF. Thus, once the voltage levels at the input of comparator 430 are the same, control signal 406 will no longer change the resistance of resistor 416.

[0040] The switch capacitance CSC ~~in FIG. 5 is~~ can be implemented as a NMOS-in-NWELL capacitor, ~~the same way for~~ similar to the capacitor 422 in the low-pass filter 402. For this design, fCLK is equal to 16 MHz, and the value of CSC is scaled to be (π C)/4 in order for R in Equation 2 to be equal to $1/(2\pi$ fc C). As a result, the desired accurate corner frequency of the low-pass filter 402 will be established.

[0042] Control signal 406 can be a digital signal so as to select one or more of the individual resistors in each respective resistor bank. In order to produce a digital control signal 406, ~~the analog-to-digital converter~~ comparator 430 can comprise a comparator 412 coupled to ~~a successive approximation register (SAR)~~ A/D converter 414. Other equivalent circuits to implement the functionality of comparator 430 for generating control signal 406 will become apparent to a person skilled in the relevant art.

[0043] In the case in which operational amplifier 412 is employed, the inventors have also discovered that the DC offset voltage of the operational amplifier produces undesirable characteristics at low VADJ voltage. To ~~compensatwoe~~ compensate for this, fCLK can be adjusted until the desired value for the LPF 402 corner frequency f_c is achieved.